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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/713,877 | 11/13/2003 | Russell Churchill | 174/274 | 1110 |

36981 7590 01/05/2007

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| EXAMINER | |
|---|---|
| WANG, TED M | |
| ART UNIT | PAPER NUMBER |
| 2611 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
|---|---|---|
| 3 MONTHS | 01/05/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/713,877 | CHURCHILL ET AL. | |
| | Examiner | Art Unit | |
| | Ted M. Wang | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,12-16 and 18-22* is/are rejected.

7)☒ Claim(s) *3-11,17 and 23-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/07/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 19-21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

- With regard claims 19-21, the limitation of "printed circuit board" as recited has not been taught in the specification of the instant application.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 12 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Myers, Jr. et al. (US 6,584,163).

- With regard claim 1, Myers, Jr. et al. discloses an apparatus that provides dynamic phase for a multi-channel communications protocol alignment comprising:

  a phase-locked loop circuit (Fig.2 element 200, Fig.4 element 200a, and column 4 lines 60-63 and column 5 lines 33-37) that receives as input a clock (Fig.2 element 145) and is operative to generate a plurality of clock phases (Fig.2 element 200 output); and

  a dynamic phase alignment circuit (Fig.2 element 130a) associated with a channel in the multi-channel communications protocol (column 4 lines 2-6) that receives as input a data signal (Fig.2 element 125) and the plurality of clock phases (Fig.2 element 200 output), wherein the dynamic phase alignment circuit is operative to select a clock phase (Fig.2 element 215 output, PHASE SELECT) from the plurality of clock phases from which to align the data signal for output to the channel (Fig.2 element 220 and output signal 135).

- With regard claim 2, Myers, Jr. et al. further discloses wherein the plurality of clock phases has a same period as the period of the clock and is equally spaced apart in phase (column 4 lines 60-63).

- With regard claim 12, Myers, Jr. et al. further discloses wherein the dynamic phase alignment circuit is further operative to perform clock recovery and wherein the data signal received as input a clock embedded in the data signals (column 4 lines 30-31).

- With regard claim 22, which is a method claim related to claim 1, all limitation is contained in claim 1. The explanation of all the limitation is already addressed in the above paragraph.

5. Claims 16 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Venkata et al. (US 2003/0052709).

- With regard claim 16, Venkata et al. discloses a programmable logic resource (Fig.1 element 10) comprising:

  programmable logic resource core circuitry (Fig.1 element 20); and

  an intellectual property block (Fig.1 element 30) that supports a multi-channel communications protocol (Fig.1 element 30, and paragraphs 3 and 25) and is coupled to the programmable logic resource core circuitry, wherein the intellectual property block comprises circuitry that accepts as input a clock (Fig.4 element 120 and paragraph 38) and data signals (Fig.4 element 52 and paragraph 38) from the programmable logic resource core circuitry and selects a phase of the clock (paragraph 38, lines 1-15) from which to align the data signals for output to each channel (paragraphs 42 and 43) in the intellectual property block.

- With regard claim 18, which is a digital processing system claim related to claim 16, Venkata et al. further discloses

  processing circuitry (Fig.14 element 1004);

  a memory coupled to the processing circuitry (Fig.1 element 1006); and

the programmable logic resource (Fig.14 element 10) as defined in claim 16 coupled to the processing circuitry and the memory.

All other limitation is contained in claim 16. The explanation of all the limitation is already addressed in the above paragraph.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Myers, Jr. et al. (US 6,584,163) in view of Kim et al. (US 2004/0161067).

- With regard claim 13-15, Myers, Jr. et al. discloses all of the subject matter as described in the above paragraph except for specifically teaching

  (a) wherein the apparatus is a programmable logic resource (claim 13),

  (b) wherein the apparatus is an application-specific standard product (claim 14),

  (c) wherein the apparatus is an application-specific integrated circuit (claim 14).

  However, Kim et al. teaches that the apparatus of the dynamic phase alignment circuit of Fig.5 may be implemented as functionality

programmed into any of a variety of circuitry, including programmable logic devices (PLDs), such as field programmable gate arrays (FPGAs) (paragraph 32 lines 1-5), standard cell-based devices (paragraph 32 lines 6-7), as well as application specific integrated circuits (ASICs) (paragraph 32 lines 7-8) in order to reduce the circuitry size so that the system cost is reduced.

Therefore, It would have been obvious to one of ordinary skill in the art at the time of the invention was made to implement the dynamic phase alignment apparatus Fig.2 130a of Myers' as functionality programmed into any of a variety of circuitry, including programmable logic devices (PLDs), such as field programmable gate arrays (FPGAs), standard cell-based devices, as well as application specific integrated circuits (ASICs) as taught by Kim et al. in order to reduce the circuitry size so that the system cost is reduced.

***Allowable Subject Matter***

8. Claims 3-11, 17 and 23-27 are objected to as being dependent upon an objected claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted M. Wang whose telephone number is 571-272-3053. The examiner can normally be reached on M-F, 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ted M Wang
Examiner
Art Unit 2611

Ted M. Wang